Abstracts

A circuit reduction technique for finding the steady-state solution of nonlinear circuits

Computing the steady-state response of large nonlinear circuits is becoming a key simulation requirement due to the rapid market growth of RF silicon integrated circuits. In this paper, we describe a nonlinear circuit reduction algorithm for finding the steady-state response. The proposed algorithm uses a congruent transformation-based technique to reduce the harmonic-balance equations into a much smaller set of equations. The main feature of the reduced circuit is that it shares with the original one a certain number of the derivatives with respect to the RF input power, steady-state analysis is then carried out on the reduced circuit instead of the original circuit.

❑ Return to main document.